What is Claimed Is:

1. Within a programmable logic device, a routing architecture to interconnect a plurality of function blocks, comprising:

a plurality of wires of the routing architecture;

a first subset of the plurality of wires oriented in a first and second direction having a first logical length; and

a second subset of the plurality of wires oriented in another first and second direction having different logical lengths,

wherein the first and second subset of the plurality of wires oriented in their respective first and second directions correspond to each other.

2. The routing architecture of claim 1 wherein the second subset of the plurality of wires has a physical length that is substantially the same as an electrically optimum physical length or an adjustment of the electrically optimum physical length to account for non-electrical considerations.

3. The routing architecture of claim 2 wherein the non-electrical considerations include at least one of the routing efficiency of the wire at the electrically optimum physical length and the pattern of connections to the wire.

4. The routing architecture of claim 1 wherein a physical length of the first subset of the plurality of wires oriented in the first direction differs from a physical length of the first subset of the plurality of wires oriented in the second direction.

5. The routing architecture of claim 1 wherein the first direction is orthogonal to the second direction.

6. The routing architecture of claim 5 wherein the first direction and the second direction are any one of a horizontal direction and a vertical direction, the vertical direction and the horizontal direction, a

diagonal direction up to the right and a diagonal direction up to the left, or the diagonal direction up to the left and the diagonal direction up to the right.

7. The routing architecture of claim 1 wherein each of the plurality of function blocks are a logic array block, a memory block, an input/output block, or a multiply-accumulate block.

8. A digital system including the programmable logic device of claim 1.

9. Within a programmable logic device, a two-dimensional routing architecture to interconnect a plurality of function blocks, comprising:

a wire having a logical length that is a function of an orientation of the wire and having a physical length that is substantially the same as an electrically optimum physical length or an adjustment of the electrically optimum physical length to account for non-electrical considerations,

wherein the wire interconnects a subset of the plurality of function blocks.

10. The two-dimensional routing architecture of claim 9 wherein the non-electrical considerations include at least one of the routing efficiency of the wire at the electrically optimum physical length and the pattern of connections to the wire.

11. The two-dimensional routing architecture of claim 9 wherein the orientation of the wire is any one of a vertical direction, a horizontal direction, a diagonal direction up to the left, or a diagonal direction up to the right.

12. The two-dimensional routing architecture of claim 9 wherein each of the plurality of function blocks are a logic array block, a memory block, an input/output block, or a multiply-accumulate block.

13. The two-dimensional routing architecture of claim 9 wherein each of the plurality of function blocks has a height that differs from its width.

14. A digital system including the programmable logic device of claim 9.

15. A method to interconnect a plurality of function blocks within a programmable logic device, comprising:

determining a physical length that is electrically optimum for a wire; and

connecting the plurality of function blocks to the wire having a physical length that is substantially the same as the physical length that is electrically optimum,

wherein a logical length of the wire is a function of an orientation of the wire.

16. The method of claim 15 further comprising

adjusting the physical length to account for non-electrical considerations,

wherein connecting the plurality of function blocks is connecting to the wire having the physical length that is substantially the same as the adjusted physical length.

17. The method of claim 16 wherein the non-electrical considerations include at least one of the routing efficiency of the wire at the physical length that is electrically optimum and the pattern of connections to the wire.

18. The method of claim 15 wherein determining the physical length that is optimum for the wire includes

modeling the programmable logic device that includes the plurality of function blocks and the wire;

varying the physical length of the wire a plurality of times;

for each of the plurality of physical length variations, determining the time for a signal to traverse the wire having the particular one of the plurality of physical length variations;

for each of the plurality of times for the signal to traverse the wire having the particular one of the plurality of physical length variations, converting this time to the time for the signal to traverse one unit length; and

from the plurality of times for the signal to traverse one unit length, selecting a particular one of the plurality of times for the signal to traverse one unit length that is the least time to traverse one unit length.

19. The method of claim 15 wherein each of the plurality of function blocks are a logic array block, a memory block, an input/output block, or a multiply-accumulate block.

20. Within a programmable logic device, a two-dimensional routing architecture to interconnect a plurality of function blocks, comprising:

a first subset of a plurality of wires having a first logical length and a physical length; and

a second subset of the plurality of wires having a second logical length and a physical length that is substantially the same as the physical length of the first subset of the plurality of wires,

wherein the first logical length differs from the second logical length.

21. The two-dimensional routing architecture of claim 20 wherein the physical length of the first subset of the plurality of wires is substantially the same as an electrically optimum physical length or an adjustment of the electrically optimum physical length to account for non-electrical considerations.

22. The two-dimensional routing architecture of claim 21 wherein the non-electrical considerations include at least one of the routing efficiency of the wire at the physical length that is electrically optimum and the pattern of connections to the wire.

23. The two-dimensional routing architecture of claim 20 wherein

the first subset of the plurality of wires is oriented in a first direction and the second subset of the plurality of wires is oriented in a second direction.

24. The two-dimensional routing architecture of claim 23 further comprising

a third subset of the plurality of wires oriented in the first direction and having a third logical length that is shorter than the first logical length;

a fourth subset of the plurality of wires oriented in the second direction and having the third logical length;

a fifth subset of the plurality of wires oriented in the first direction and having a fourth logical length that is shorter than the third logical length; and

a sixth subset of the plurality of wires oriented in the second direction and having the fourth logical length,

wherein a physical length of the third subset of the plurality of wires differs from a physical length of the fourth subset of the plurality of wires and a physical length of the fifth subset of the plurality of wires differs from a physical length of the sixth subset of the plurality of wires.

25. The two-dimensional routing architecture of claim 24 wherein

the first direction is orthogonal to the second direction.

26. The two-dimensional routing architecture of claim 25 wherein

the first direction is a horizontal direction and the second direction is a vertical direction and the first logical length is 24 function blocks, the second logical length is 16 function blocks, the third logical length is 8 function blocks, and the fourth logical length is 4 function blocks.

27. The two-dimensional routing architecture of claim 24 wherein

a first one of the plurality of wires oriented in a stagger direction and having a first starting point, a first ending point, and a stagger logical length; and

a second one of the plurality of wires oriented in the stagger direction and having a second starting point, a second ending point, and the stagger logical length,

wherein if the stagger direction is a horizontal direction then the first starting point is offset from the second starting point and the first ending point is offset from the second ending point by a fixed number of a plurality of columns of function blocks of an array of function blocks, or if the stagger direction is a vertical direction then the first starting point is offset from the second starting point and the first ending point is offset from the second ending point by the fixed number of a plurality of rows of function blocks of the array of function blocks.

28. The two-dimensional routing architecture of claim 27 wherein the fixed number is any one of zero, one, or two.

29. The two-dimensional routing architecture of claim 24 wherein the first direction is a horizontal direction and

a first wire of a particular one of the first subset of the plurality of wires, the third subset of the plurality of wires, or the fifth subset of the plurality of wires and having a first starting point;

a first driver having an output, the output coupled to the first wire at the first starting point, to drive a first signal on the first wire to the right;

a second wire of the particular one of the subsets having a second starting point; and

a second driver having an output, the output coupled to the second wire at the second starting point, to drive a second signal on the second wire to the left.

30. The two-dimensional routing architecture of claim 24 wherein the second direction is a vertical direction and

a first wire of a particular one of the second subset of the plurality of wires, the fourth subset of the plurality of wires, or the sixth subset of the plurality of wires and having a first starting point;

a first driver having an output, the output coupled to the first wire at the first starting point, to drive a first signal on the first wire in the upward direction;

a second wire of the particular one of the subsets having a second starting point; and

a second driver having an output, the output coupled to the second wire at the second starting point, to drive a second signal on the second wire in the downward direction.

31. The two-dimensional routing architecture of claim 24 wherein

a first one of the plurality of wires oriented in a stitching direction and having a signal flow direction, a stitching logical length, a first starting point, and a first ending point that is the stitching logical length away in the signal flow direction from the first starting point;

a second one of the plurality of wires oriented in the stitching direction and having the signal flow direction, the stitching logical length, a second starting point, and a second ending point that is the stitching logical length away in the signal flow direction from the second starting point; and

a driver having an input and an output, the input coupled to the first one of the plurality of wires at a position ranging from the first starting point to the first ending point and the output coupled to the second one of the plurality of wires at the second starting point, to drive the signal on the second one of

the plurality of wires in the signal flow direction from the second starting point to the second ending point.

32. The two-dimensional routing architecture of claim 31 wherein

the input of the second driver is coupled to the first one of the plurality of wires at the first ending point.

33. The two-dimensional routing architecture of claim 24 wherein

a first one of the fifth subset of the plurality of wires oriented in the first direction is coupled to at least one of a first one of the first subset of the plurality of wires oriented in the first direction, a first one of the second subset of the plurality of wires oriented in the second direction, a first one of the sixth subset of the plurality of wires oriented in the second direction, and a particular one of the plurality of function blocks spanned by the first one of the fifth subset of the plurality of wires;

a first one of the third subset of the plurality of wires oriented in the first direction is coupled to at least one of a first one of the fourth subset of the plurality of wires oriented in the second direction, and a particular one of the plurality of function blocks spanned by the first one of the third subset of the plurality of wires;

a second one of the first subset of the plurality of wires oriented in the first direction is coupled to at least one of a second one of the fifth subset of the plurality of wires oriented in the first direction, a second one of the second subset of the plurality of wires oriented in the second direction, and a second one of the sixth subset of the plurality of wires oriented in the second direction;

a third one of the sixth subset of the plurality of wires oriented in the second direction is coupled to at least one of a third one of the first subset of the plurality of wires oriented in the first direction, a third one of the fifth subset of the plurality of wires oriented in the first direction, a third one of the second subset of the plurality of wires oriented in the second direction, and a particular one of the plurality of function blocks spanned by the third one of the sixth subset of the plurality of wires;

a second one of the fourth subset of the plurality of wires oriented in the second direction is coupled to at least one of a second one of the third subset of the plurality of wires oriented in the first direction, and a particular one of the plurality of function blocks spanned by the second one of the fourth subset of the plurality of wires; and

a fourth one of the second subset of the plurality of wires oriented in the second direction is coupled to at least one of a fourth one of the first subset of the plurality of wires oriented in the first direction, a fourth one of the fifth subset of the plurality of wires oriented in the first direction, a fourth one of the sixth subset of the plurality of wires oriented in the second direction, and a particular one of the plurality of function blocks spanned by the fourth one of the second subset of the plurality of wires.

34. The two-dimensional routing architecture of claim 24 wherein the two-dimensional routing architecture includes a plurality of rows and a plurality of columns of function blocks and

a first driver corresponding to a first one of the plurality of columns of function blocks and having at least one input and an output, the at least one input coupled to at least one of a first one of the first subset of the plurality of wires, a first one of the second subset of the plurality of wires, a first one of the sixth subset of the plurality of wires, an output of the first one of the plurality of columns of function blocks, and an output of a second one of the plurality of columns of function blocks that is adjacent to the first one of the plurality of columns of function blocks, and the output of the first driver coupled to a first one of the fifth subset of the plurality of wires;

a second driver corresponding to a third one of the plurality of columns of function blocks and having at least one input and an output, the at least one input coupled to at least one of a first one of the fourth subset of the plurality of wires, an output of the third one of the plurality of columns of function blocks, and an output of a fourth one of the plurality of columns of function blocks that is adjacent to the third one of the plurality of columns of function blocks, and the output of the second driver coupled to a first one of the third subset of the plurality of wires;

a third driver having at least one input and an output, the at least one input coupled to at least one of a second one of the fifth subset of the plurality of wires, a second one of the second subset of the plurality of wires, and a second one of the sixth subset of the plurality of wires, and the output of the third driver coupled to a second one of the first subset of the plurality of wires;

a fourth driver corresponding to a first one of the plurality of rows of function blocks and having at least one input and an output, the at least one input coupled to at least one of a third one of the first subset of the plurality of wires, a third one of the fifth subset of the plurality of wires, a third one of the second subset of the plurality of wires, an output of the first one of the plurality of rows of function blocks, and an output of a second one of the plurality of rows of function blocks that is adjacent to the

first one of the plurality of rows of function blocks, and the output of the fourth driver coupled to a third one of the sixth subset of the plurality of wires;

a fifth driver corresponding to a third one of the plurality of rows of function blocks and having at least one input and an output, the at least one input coupled to a second one of the third subset of the plurality of wires, an output of the third one of the plurality of rows of function blocks, and an output of a fourth one of the plurality of rows of function blocks that is adjacent to the third one of the plurality of rows of function blocks, and the output of the fifth driver coupled to a second one of the fourth subset of the plurality of wires; and

a sixth driver having at least one input and an output, the at least one input coupled to a fourth one of the first subset of the plurality of wires, a fourth one of the fifth subset of the plurality of wires, and a fourth one of the sixth subset of the plurality of wires, and the output of the sixth driver coupled to a fourth one of the second subset of the plurality of wires.

35. The two-dimensional routing architecture of claim 24 wherein

the first subset of the plurality of wires is wider than the third subset of the plurality of wires, the third subset of the plurality of wires is wider than the fifth subset of the plurality of wires, the second subset of the plurality of wires is wider than the fourth subset of the plurality of wires, and the fourth subset of the plurality of wires is wider than the sixth subset of the plurality of wires.